

What is claimed is:

1 1. An apparatus for performing encoding operations, the  
2 apparatus comprising:  
3 memory including a set of memory locations for storing  
4 L sets of Z-bit vectors, where Z is a positive integer greater  
5 than one and L is a positive integer;  
6 a vector unit operation processor including an  
7 accumulator and output device for passing computed Z-bit vector  
8 to the said memory in response to operation instructions; and  
9 a switching device coupled to the memory and to the  
10 vector unit operation processor, the switching device for  
11 passing a Z-bit vector between said memory and said vector unit  
12 operation processor in response to switch control information.

1 2. The apparatus of claim 1, further comprising:  
2 an ordering control module coupled to said memory for  
3 generating read and write indices; and  
4 an operation control module coupled to said vector  
5 unit operation processor for generating unit operation  
6 instructions.

1 3. The apparatus of claim 2, wherein the ordering control  
2 module is further coupled to said switch device for generating  
3 said switch control information used to control the switching of  
4 said at least one vector.

1 4. The apparatus of claim 1, wherein the switching device  
2 includes circuitry for performing a vector rotation operation to  
3 generate a rotated vector.

1 5. The apparatus of claim 2, wherein the ordering control  
2 module stores information on the order of vectors are to be read  
3 out of the memory and information on the order of vectors are to  
4 be written into the memory.

1 6. The apparatus of claim 2, wherein the ordering control  
2 module further stores information on the rotation to be  
3 performed on the read-out vectors from said memory by said  
4 switch.

1 7. The apparatus of claim 2, wherein the ordering control  
2 module sequentially generates index identifiers, each identifier  
3 controlling the memory to access memory locations corresponding  
4 to a vector as part of a single SIMD instruction.

1 8. The apparatus of claim 7, wherein each identifier is a  
2 single memory address.

1 9. The apparatus of claim 2, wherein said operation control  
2 module stores operation instructions, each instruction  
3 controlling the operation at said vector unit operation  
4 processor.

1 10. The apparatus of claim 9, wherein the operation control  
2 module sequentially generates operation instructions, each  
3 instruction controlling said vector unit operation processor to  
4 perform instructed operations.

1 11. The apparatus of claim 2, further comprising an encoder  
2 control module coupled to said ordering control module, the  
3 encoder control module including means for supplying information  
4 to said ordering control module used to control the order in  
5 which each of the L vectors is to be read out of said memory,  
6 their associated rotations, and the order to be written into  
7 said memory.

1 12. The apparatus of claim 11, wherein the encoder control  
2 device is further coupled to said operation control module, the  
3 encoder control device including means for supplying information

4 to said operation control module used to generate operation  
5 instructions.

1 13. A method of performing encoding operations, the method  
2 comprising:

3 storing L sets of Z-bit vectors in a memory device,  
4 where Z is a positive integer greater than one and L is a  
5 positive integer;

6 reading one of said sets of Z bit vectors from said  
7 stored L sets of Z bit vectors;

8 rotating the bits in said read one of said Z bit  
9 vectors; and

10 operating a vector unit processor to perform a  
11 plurality of combining operations to combine the bits of the  
12 rotated Z bit vector with a Z-bit vector stored in said vector  
13 unit processor to generate a new Z-bit vector.

1 14. The method of claim 13, further comprising:

2 storing said new Z bit vector in said memory device in the  
3 place of one of the stored L sets of Z bit vectors.

1 15. The method of claim 14, wherein said combining operations  
2 performed by said vector unit processor are exclusive OR  
3 operations.

1 16. The method of claim 15 wherein said encoding method is a  
2 low density parity check encoding method.

1 17. The method of claim 14, further comprising:

2 executing a set of stored machine executable  
3 instructions to control the rotation of the read Z bit vector.

1 18. The method of claim 14, further comprising:

2           using the executed set of stored machine executable  
3 instructions to determine which one of said sets of stored Z bit  
4 vectors is to be read from memory.

1 19. The method of claim 14, further comprising:

2           using the executed set of stored machine executable  
3 instructions to determine when one of said sets of stored Z bit  
4 vectors is to be read from memory.

1 20. The method of claim 19, further comprising:

2           using the executed set of stored machine executable  
3 instructions to determine which one of the stored L sets of Z  
4 bit vectors is to be replaced by storing the new Z bit vector in  
5 said memory device.

1 21. The method of claim 19, further comprising:

2           resetting the Z bit vector stored in said vector unit  
3 processor at the same time said new Z bit vector is stored.

1 22. The method of claim 14, further comprising:

2           resetting the Z bit vector stored in said vector unit  
3 processor at the same time said new Z bit vector is stored.

1 23. The method of claim 14, further comprising:

2           using the executed set of stored machine executable  
3 instructions to determine which one of the stored L sets of Z  
4 bit vectors is to be replaced by storing the new Z bit vector in  
5 said memory device.

1 24. A method of performing encoding operations, the method  
2 comprising:

3           storing L sets of Z-bit vectors in a memory device,  
4 where Z is a positive integer greater than one and L is a  
5 positive integer;

6           reading one of said sets of Z bit vectors from said  
7 stored L sets of Z bit vectors;  
8           operating a vector unit processor to perform a  
9 plurality of combining operations to combine the bits of the  
10 rotated Z bit vector with a Z-bit vector stored in said vector  
11 unit processor to generate a new Z-bit vector;  
12           rotating the bits in said new Z bit vector; and  
13           storing said rotated new Z bit vector in said memory  
14 device in the place of one of the stored L sets of Z bit  
15 vectors.

1   25. The method of claim 24,  
2       wherein said combining operations performed by said vector  
3 unit processor are exclusive OR operations; and  
4       wherein said encoding method is a low density parity check  
5 encoding method.

1   26. The method of claim 25, further comprising:  
2       executing a set of stored machine executable  
3 instructions to control the rotation of the read Z bit vector  
4 and to determine which one of the stored L sets of Z bit vectors  
5 is to be replaced by storing said rotated new Z bit vector in  
6 said memory device.